IN THE CLAIMS

1. (previously presented) A comparator unit comprising:

a first amplifier stage including a differential amplifier having a pair of input nodes and a pair of output nodes, a switch connected across the pair of output nodes, and a non-linear load connected across the pair of output nodes; and

a second amplifier stage coupled to the pair of output nodes, the second amplifier stage including an input pair of isolated gate field-effect transistors and a cross-coupled pair of isolated gate field-effect transistors, wherein each of the cross-coupled pair of isolated gate field-effect transistors is coupled in parallel with a corresponding one of the input pair of isolated gate field-effect transistors.

2. (original) The comparator unit of claim 1, wherein the differential amplifier comprises a pair of differential pairs of isolated gate field-effect transistors.

3. (original) The comparator unit of claim 2, wherein the switch comprises an electronically controllable switch.

4. (original) The comparator unit of claim 3, wherein the electronically controllable switch comprises an isolated gate field-effect transistor.

5. (original) The comparator unit of claim 4, wherein the non-linear load comprises a pair of cross-coupled isolated gate field-effect transistors.

6. (original) The comparator unit of claim 5, wherein each transistor in the pair of cross-coupled isolated gate field-effect transistors comprises an n-channel isolated gate field-effect transistor.

7. (original) The comparator unit of claim 1, wherein the second amplifier stage comprises a non-linear amplifier.

8. (previously presented) The comparator unit of claim 7, wherein the second amplifier stage includes a pair of second stage output nodes and a switch connected across the pair of second stage output nodes.

9. (original) The comparator unit of claim 1, wherein the differential amplifier comprises a differential pair of isolated gate field-effect transistors.

10.-34. (canceled)

35. (previously presented) A comparator unit comprising:

a first amplifier stage including a differential amplifier having a pair of input nodes and a pair of output nodes, a switch connected across the pair of output nodes, and a non-linear load connected across the pair of output nodes; and

a second amplifier stage including an input pair of isolated gate field-effect transistors and a cross-coupled pair of isolated gate field-effect transistors, the input pair of isolated gate field-effect transistors having a pair of gates, wherein the pair of gates are coupled to the pair of output nodes and each of the cross-coupled pair of isolated gate field-effect transistors is coupled in parallel with a corresponding one of the input pair of isolated gate field-effect transistors.

36. (previously presented) The comparator unit of claim 35, wherein the differential amplifier comprises a pair of differential pairs of isolated gate field-effect transistors.

37. (previously presented) The comparator unit of claim 36, wherein the switch comprises an electronically controllable switch.

38. (previously presented) The comparator unit of claim 37, wherein the electronically controllable switch comprises an isolated gate field-effect transistor.

39. (previously presented) The comparator unit of claim 38, wherein the non-linear load comprises a pair of cross-coupled isolated gate field-effect transistors.

40. (previously presented) The comparator unit of claim 39, wherein each transistor in the pair of cross-coupled isolated gate field-effect transistors comprises an n-channel isolated gate field-effect transistor.

41. (previously presented) The comparator unit of claim 35, wherein the second amplifier stage comprises a non-linear amplifier.

42. (previously presented) The comparator unit of claim 41, wherein the second amplifier stage includes a pair of second stage output nodes and a switch connected across the pair of second stage output nodes.

43. (previously presented) The comparator unit of claim 35, wherein the differential amplifier comprises a differential pair of isolated gate field-effect transistors.